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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/241,177	02/01/1999	SALMAN AKRAM	3638US-(98-0	8330

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JAMES R DUZAN
TRASK BRITT & ROSSA
P O BOX 2550
SALT LAKE CITY, UT 84110

EXAMINER	
NOVACEK, CHRISTY L	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 04/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/241,177	AKRAM ET AL.	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this communication appears on th cover sheet with th correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39 and 44-53* is/are pending in the application.

4a) Of the above claim(s) *1-31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *32-39 and 44-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *24 January 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to the amendment filed January 24, 2002.

Election/Restrictions

This application contains claims 1-31 drawn to an invention nonelected without traverse. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Drawings

The proposed drawing corrections of Figures 5-8, filed on January 24, 2002, have been approved.

The proposed drawing corrections of Figures 7 and 8, filed on December 18, 2000, have been approved.

The proposed drawing correction of Figure 9, filed on December 18, 2000, has been **disapproved**. As stated in the previous Office Action, the proposed correction to Figure 9 shows the reference sign "30B" pointing to the middle through-slot and reference sign "30C" pointing to one of the outer through-slots, while Figures 3, 5, 6 and 7, as well as the specification on page 6, line 28-page 7, line 4, disclose that the middle through-slot is designated as "30C" and the outer through-slots are labeled "30A" and "30B".

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because Figure 10 shows the reference sign "30B" pointing to the middle through-slot and reference sign "30C" pointing to one of the outer through-slots, while Figures 3, 5, 6 and 7, as well as the specification

on page 6, line 28-page 7, line 4, disclose that the middle through-slot is designated as "30C" and the outer through-slots are labeled "30A" and "30B". Correction is required.

A proper drawing correction or corrected drawings are required in reply to the Office action to avoid **abandonment** of the application. The correction to the drawings will not be held in abeyance.

Response to Amendment

The amendment of the specification is sufficient to overcome the rejection of claims 35-37 and 47-49 under 35 U.S.C. 112, first paragraph as stated in the previous Office Action. Therefore, this rejection is withdrawn.

The amendment of the claims 32 and 44 is sufficient to overcome the rejection of claims 32-39 and 44-53 under 35 U.S.C. 112, second paragraph as stated in the previous Office Action. Therefore, this rejection is withdrawn.

Claim Objections

Claim 32 is objected to because of the following informalities: Lines 7-8 of claim 32 recite, "one each said first side and second side of said substrate". This typographical error may be corrected by replacing "one each" with "on each of". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 32-37, 39, 44-49 and 51-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. (US 5,998,860, previously cited) in view of Akram et al. (US 5,811,879, previously cited) and Swamy et al. (US 5,835,357, previously cited).

In reference to claims 32, 44 and 52 and 53, Chan discloses a plurality of semiconductor dice (50) each having an active surface and a plurality of bond pads (120). A planar substrate (70) has opposing first and second sides (92, 94) and at least three elongate through-slots (86) extending from the first side to the second side. A pattern of conduits (118) (inherently electrical conductors) is formed on each side of the substrate and is connected to terminal contacts (82) that are adjacent to the through-slots on the substrate. The terminal contacts connect the bond pads of the dice the conduits which, in turn, connect to an input/output connector (104). The active surfaces of some of the dice are attached to the first side of the substrate and the bond pads of the dice are aligned with alternate through-slots for access from the second side of the substrate. The active surfaces of some of the other dice are attached to the second side of the substrate and the bond pads of these dice are also aligned with alternate through-slots for access from the first side of the substrate. The bond pads of the dice are wire-bonded to the terminal contacts adjacent the through-slots. See Fig. 1 and 2 and col. 4, ln. 37-63.

Chan does not specifically disclose that the conductor patterns on each side of the substrate are connected by vias in the substrate. Chan shows in Figure 1 that the dice mounted to the first side of the circuit board are electrically connected to the surface of the second side of the circuit board by wires. The dice mounted to the second side of the circuit board are electrically connected to the surface of the first side of the circuit board by wires. In order for the dice on both sides of the package to be electrically connected to one another, there must be connections present in the form of internal circuitry within the circuit board, as is conventional in the art.

Akram discloses a multichip package similar to that of Chan in which the internal circuitry that is connected to the electrical conductor patterns on the exterior surfaces of the board is specifically disclosed as being formed of vias (col. 3, ln. 58-61). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the inherent internal circuitry of conductive vias, because, in the absence of the disclosure of any particular interconnection method, one of ordinary skill in the art would look to use a conventional process, such as that of Akram, to form the required circuitry.

Chan discloses an input/output connector of tabs (104) formed on the edge of the substrate, which are used to mount the package vertically (col. 4, ln. 58-61). Chan does not disclose other types of connectors. Akram discloses a multichip IC package similar to that of Chan, in which the input/output connectors are formed of tabs in one embodiment, and are formed of a ball-grid array at the peripheral area of the board in another embodiment (col. 6, ln. 39-46). In reference to using ball-grid array (BGA) connectors to form electrical connections between an IC package and higher-level circuitry, Swamy states, "Those of ordinary skill in the art are familiar with the structure and advantages of such connectors." (col. 4, ln. 4-7). At the time of the invention, one of ordinary skill in the art would have found it obvious to substitute ball-grid array connectors for the tab connectors of Chan as a matter of design choice because, as is disclosed by Akram and Swamy, ball-grid array connectors and tabs are conventional art-recognized equivalents for the purpose forming IC package connections.

In reference to claims 33 and 45, Chan discloses that the through-slots are made by forming an elongate stepped surface in the through-slots (Fig. 2-4).

In reference to claims 34 and 46, Chan discloses that the conductive connection terminals are formed on the elongate stepped surface (Fig. 3-4).

In reference to claims 35 and 47, Chan discloses that a glob-top material (90) is inserted into each through-slot to encapsulate the wires (Fig. 1; col. 5, ln. 49-59). This material is disclosed to be a resin which is, inherently, flowable and hardenable.

In reference to claims 36 and 48, Chan discloses a hardenable polymeric material is inserted into each through-slot (Fig. 1; col. 5, ln. 49-59).

In reference to claims 37 and 49, as can been seen in Figure 1, Chan discloses that the glob-top material is inserted to extend outwardly between the edges of at least two die proximate each side of the through-slots.

In reference to claims 39 and 51, Chan discloses that the polymeric glob-top material is also used to encapsulate/seal the die (Fig. 1, 5; col. 6, ln. 54-58).

Claims 32, 38, 44, 50, 52, and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiu (US 5,243,497, previously cited) in view of Swamy et al.

In reference to claims 32, 44, 52 and 53, Chiu discloses a plurality of semiconductor dice (32) each having an active surface and a plurality of bond pads (35). A planar substrate (31) has opposing first and second sides and at least three elongate through-slots (33) extending from the first side to the second side. A pattern of circuitry (inherently electrical conductors) connected to terminal contacts (34) is adjacent to the through-slots on the substrate (col. 2, ln. 2-9). Chiu does not specifically disclose forming a circuitry pattern on both the first and second sides of the board (col. 2, ln. 7-15). However, according to Chiu, a short bond wire connects each semiconductor die on both sides of the substrate to the circuitry on the circuit board. This would inherently require a pattern of circuitry to be on both sides of the board.

The active surfaces of some of the dice are attached to the first side of the substrate and the bond pads of the dice are aligned with alternate through-slots for access from the second side of the substrate. The active surfaces of some of the other dice are attached to the second side of the substrate and the bond pads of these dice are also aligned with alternate through-slots for access from the first side of the substrate. The bond pads of the dice are wire-bonded to the terminal contacts adjacent the through-slots. See Fig. 3-5 and col. 2, ln. 2-9 and ln. 33-47. Chiu does not disclose the circuit board (substrate) to have an input/output connector. However, the circuit board must inherently have an input/output connector so that the semiconductor dice can be electrically accessed by the hardware that it is connected to. Similarly, the input/output connector must also inherently be connected to the terminal contacts (34) in order to be electrically connected to the dice. At the time of the invention, it would have been obvious to one of ordinary skill in the art, to form the inherent input/output connector such that it is connected to the terminal contacts because the terminal contacts are connected to the semiconductor dice which must be connected to an electrical source in order to function.

Chiu does not disclose connecting the conductor patterns with vias through the substrate. However, in Figure 4, Chiu shows that the dice mounted to the first side of the circuit board are electrically connected to the surface of the second side of the circuit board by wires. The dice mounted to the second side of the circuit board are electrically connected to the surface of the first side of the circuit board by wires. In order for the dice on both sides of the package to be electrically connected to one another, there must be connections present in the form of internal circuitry within the circuit board, as is conventional in the art. Swamy discloses an IC package in which the internal circuitry that is connected to the electrical conductor patterns on the exterior surfaces of the board are connected by vias (Fig. 3, col. 6, ln. 17-20). At the time of the

invention, it would have been obvious to one of ordinary skill in the art to form the inherent internal circuitry of conductive vias because it is well known in the art to provide vias in a substrate in order to connect circuitry on one surface of a circuit board to circuitry on the opposite surface of the board.

Chiu does not disclose an input/output connector connected to the package. However, as stated above, an integrated circuit package must inherently have some form of an input/output connector in order to electrically access the attached semiconductor dice. Swamy discloses using ball-grid array (BGA) connectors to form electrical connections between an IC package and higher-level circuitry. In reference to these BGA connectors, Swamy states, "Those of ordinary skill in the art are familiar with the structure and advantages of such connectors." (col. 4, ln. 4-7). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use a ball-grid array to form the required input/output connectors of the package of Chiu because, in the absence of the disclosure of any particular type of connector, one of ordinary skill in the art would look to use a conventional connector, such as the ball-grid array, to form the required structure. Furthermore, it would have been obvious to one of ordinary skill in the art to form the ball-grid array connectors on the peripheral area of the substrate of Chiu because, as shown in Fig. 3, the peripheral area is the only surface of the board that is exposed (not covered with dice) and available for connectors to be attached thereto.

In reference to claims 38 and 50, Chiu discloses that the semiconductor dice is electrically tested following wire-bonding but prior to any wire encapsulation (col. 2, ln. 31-32).

Claims 35-37, 39, 47-49 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiu in view of Swamy et al., as applied to claims 32 and 44 above, and further in view of Chan et al.

In reference to claims 35, 36, 47 and 48, Chiu discloses that a glob-top material (36) is inserted into each through-slot to encapsulate the wires, but does not disclose what type of encapsulant is used (Fig. 4; col. 2, ln. 31-32). However, encapsulants used to protect wires in an integrated circuit package typically comprise a flowable, hardenable polymeric material, such as a resin, as is disclosed by Chan (Fig. 1; col. 5, ln. 49-59). The encapsulant must be flowable so that the material can completely surround and seal the wires while also being hardenable so that it can protect the wires from breakage. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use a hardenable, flowable polymeric material, such as a resin, to encapsulate the wires of Chiu because, in the absence of the disclosure of any particular material, one of ordinary skill in the art would look to use a conventional material, such as a resin disclosed by Chan, to form the encapsulant.

In reference to claims 37 and 49, as can been seen in Figure 4 of Chiu, the glob-top material is inserted to extend outwardly between the edges of at least two die proximate each side of the through-slots.

In reference to claims 39 and 51, Chiu discloses encapsulating the wires but not the semiconductor dice (Fig. 4; col. 2, ln. 31-32). Chan's IC package has both the semiconductor dice and the wires encapsulated to hermetically protect them from moisture (Fig. 1 and 5, col. 6, ln. 54-58; col. 7, ln. 33-35). At the time of the invention, it would have been obvious to one of ordinary skill in the art to encapsulate the dice of Chiu in addition to the wires because, as is well

known in the art, semiconductor dice can be fatally damaged by moisture, and by hermetically encapsulating them, the dice can be protected against malfunction.

Response to Arguments

Applicant's arguments filed January 24, 2002 have been fully considered but they are not persuasive.

Applicants' argue that claims 32 and 44 are patentable over Chan or Chiu because neither Chan nor Chiu discloses forming ball-grid array (BGA) connectors on the substrate of the package. Chan discloses forming electrical connectors of a tab structure instead of BGA connectors. The Akram reference shows that an IC package may have electrical connectors of either a tab structure or a BGA structure, with the choice of which type of connectors to use based upon the type of higher-level circuitry that the package is being connected to. Chiu does not disclose any electrical connectors on the IC package of his invention. However, as stated above, such connectors must be present in order for the package to be electrically connected to a power source. The use of BGA electrical connectors is conventional and well known in the art. This is supported by Swamy, who, in reference to BGA connectors, states, "Those of ordinary skill in the art are familiar with the structure and advantages of such connectors." Therefore, the use of such BGA connectors on the IC package of Applicants' invention does not patentably distinguish it from the prior art.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (703) 308-5840. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Michael Trinh
Primary Examiner

CLN
April 11, 2002